

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
Tomohiko IMADA et al.)
Serial No. 10/617,931) Art Unit: 2825
Filed: July 11, 2003) Examiner: Do, Thuan V.
For: System, Method and Computer Program)
Product for Designing Connecting)
Terminals of Semiconductor Device) Attorney Docket No.: 44471/287602

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Lesley L. Andrew: /Lesley L. Andrew/

Date: February 7, 2008

COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Notice of Allowability mailed November 19, 2007 included a statement of reasons for allowance. The reasons for allowance cite particular claim elements from Claim 1 as not taught by the prior art of record. In particular the reasons for allowance state:

The prior art of record does not teach a verifier configured to verify whether the power supply cells, I/O signal cells, and first and second connecting nets violate predetermined design rules with the combination of all other features corresponding to each independent claim.

Comments on Examiner's Statement of Reasons for Allowance

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Claim 6 recites "verifying whether the power supply cells, I/O signal cells, and first and second connecting nets violate predetermined design rules" and Claim 10 recites "instructions configured to verify whether the power supply cells, I/O signal cells, and first and second connecting nets violate predetermined design rules."

To the extent that the Examiner's reasons for allowance suggest or state that certain limitations or combinations are not found in the prior art and imply that all of the independent claims recite particular claim elements, it is noted that "the record as a whole" must be considered as a supplement to the statement of reasons for allowance, and to the extent that the record is clear and complete, it shall control the interpretation of any and all claims.

Respectfully submitted,



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